IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Cline *et al.* Examiner: Chen, Eric Brice

Serial No.:10/711,953 Art Unit: 1765

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Title: **DEEP TRENCH FORMATION IN SEMICONDUCTOR DEVICE FABRICATION**

Commissioner for Patents
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AMENDEMENT AFTER FINAL REJECTION

Please enter this amendment that places the claims in conditions for allowance suggested by the Examiner.

In the Claims:

Please cancel claims 1, 2, 12, and 13. Please amend claims 3, 6, 7, and 9. The claims are as follows:

1. (Canceled).

2. (Canceled).

3. (Currently amended) ~~The method of claim 1,~~ A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of deep trenches, wherein forming each trench of the first plurality of deep trenches includes the steps of:

(i) providing a semiconductor substrate,

(ii) forming a hard mask layer on top of the semiconductor substrate,

(iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters,

(iv) etching a deep trench in the substrate via the hard mask opening; and

(b) determining a first yield of the first plurality of deep trenches; and

(c) if the first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of

etching the bottom portion of the hard mask opening is performed according to a second set of etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches,

wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, the step of etching the bottom portion of the hard mask opening has a lower degree of anisotropy than that associated with the a trench of the first plurality of deep trenches.

4. (Original) The method of claim 3, wherein the lower degree of anisotropy is achieved by reducing a flow rate of a noble gas.

5. (Original) The method of claim 4, wherein the noble gas comprises argon (Ar).

6. (Currently amended) ~~The method of claim 1,~~ A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of deep trenches, wherein forming each trench of the first plurality of deep trenches includes the steps of:

(i) providing a semiconductor substrate,

(ii) forming a hard mask layer on top of the semiconductor substrate,

(iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters,

(iv) etching a deep trench in the substrate via the hard mask opening; and

(b) determining a first yield of the first plurality of deep trenches; and

(c) if the first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a second set of etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches,

wherein the bottom portion of the hard mask opening has a greater lateral width than a top portion of the hard mask opening.

7. (Currently amended) ~~The method of claim 1,~~ A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of deep trenches, wherein forming each trench of the first plurality of deep trenches includes the steps of:

(i) providing a semiconductor substrate,

(ii) forming a hard mask layer on top of the semiconductor substrate,

(iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters,

(iv) etching a deep trench in the substrate via the hard mask opening; and

(b) determining a first yield of the first plurality of deep trenches; and

(c) if the first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a second set of etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches,

wherein the step of forming the hard mask layer comprises the steps of:

forming a pad oxide layer on top of the semiconductor substrate, and

forming a nitride layer on top of the pad oxide layer,

wherein, in the formation of the first plurality of deep trenches, a first side wall of the bottom portion of the hard mask opening associated with the nitride layer has a first height,

wherein, in the formation of the second plurality of deep trenches, a second side wall of the bottom portion of the hard mask opening associated with the nitride layer has a second height, and

wherein the first height is greater than the second height.

8. (Original) The method of claim 7, wherein the step of forming the hard mask layer further comprises the steps of:

forming a BSG (borosilicate glass) layer on top of the nitride layer; and

forming an ARC (anti-reflective coating) layer on top of the BSG layer.

9. (Currently amended) ~~The method of claim 1,~~ A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of deep trenches, wherein forming each trench of the first plurality of deep trenches includes the steps of:

(i) providing a semiconductor substrate,

(ii) forming a hard mask layer on top of the semiconductor substrate,

(iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters,

(iv) etching a deep trench in the substrate via the hard mask opening; and

(b) determining a first yield of the first plurality of deep trenches; and

(c) if the first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a second set of

etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches,

wherein the second set of etching parameters are further adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, the bottom portion of the hard mask opening has a rounder bottom corner than that corresponding to a trench of the first plurality of deep trenches.

10. (Original) The method of claim 9, wherein the rounder bottom corner is achieved by reducing a flow rate of a noble gas.

11. (Original) The method of claim 10, wherein the noble gas comprises argon (Ar).

12. (Canceled).

13. (Canceled).

14. (Previously presented) A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming a hard mask layer on top of the semiconductor substrate;

(c) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening,

wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening such that a side wall of the bottom portion of the hard mask opening is substantially vertical, and such that the bottom portion of the hard mask opening has a greater lateral width than a top portion of the hard mask opening; and

(d) etching a deep trench in the substrate via the hard mask opening.

15. (Original) The method of claim 14, further comprising a de-polymerization step so as to remove polymers from a surface of the semiconductor structure after the step of etching the hard mask opening and before the step of etching the deep trench.

16. (Original) The method of claim 14, wherein the step of etching the bottom portion of the hard mask opening has a degree of anisotropy lower than a predetermined degree of anisotropy associated with a side wall angle which is considered substantially vertical.

17. (Canceled)

18. (Withdrawn) A semiconductor structure, comprising:

(a) a semiconductor substrate;

(b) a hard mask layer on top of the semiconductor substrate; and

(c) a hard mask layer opening in the hard mask layer,

wherein the semiconductor substrate is exposed to the atmosphere through the hard mask layer opening,

wherein the hard mask layer opening comprises top and bottom portions,

wherein the bottom portion is beneath the top portion, and

wherein a side wall of the bottom portion of the hard mask layer opening is substantially vertical.

19. (Withdrawn) The structure of claim 18, wherein the hard mask layer comprises:

a pad oxide on top of the semiconductor substrate; and

a nitride layer on top of the pad oxide layer,

wherein the nitride layer and the pad oxide layer are exposed to the atmosphere on a side wall of the bottom portion of the hard mask layer opening.

20. (Withdrawn) The structure of claim 18, wherein the bottom portion of the hard mask opening has a greater lateral width than the top portion of the hard mask opening.

REMARKS

This amendment places the claims in conditions for allowance suggested by the Examiner by (i) canceling all rejected claims 1, 2, 12, and 13, and (ii) rewriting objected-to claims 3, 6, 7, and 9 in independent forms including all of the limitations of base claim 1.

Applicants thank the Examiner for allowing claims 14-16.

CONCLUSION

Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

Date: 06/21/2006

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